Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **ADJ**
2. **Vin**
3. **VOUT**
4. **VOUT**
5. **VIN**
6. **VOUT**
7. **N/C**
8. **N/C**
9. **N/C**
10. **N/C**
11. **N/C**

**.086”**

**4 3**

**6**

**5 2**

**7**

**8**

**9**

**10**

**11**

**1**

**SiS137K**

**MASK**

**REF**

**106”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VIN**

**Mask Ref: SiS137**

**APPROVED BY: DK DIE SIZE .086” X .106” DATE: 6/27/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: LM137**

**DG 10.1.2**

#### Rev B, 7/19/02